Application Note

Document No.: AN1179

GALT62120 Application Guidelines

Version: V1.0

1 Introduction

GALT62120 is an automotive-grade 12-channel high-side LED driver launched by Geehy. It complies with the AEC-Q100 Grade 1 standard (operating temperature range -40°C to 125°C) and integrates a serial communication protocol, complete fault diagnosis mechanisms, a programmable watchdog, and non-volatile EEPROM. It is designed for automotive exterior lighting (tail lights, turn signals, daytime running lights), interior lighting, and pixel lights. The maximum output current per channel is 100mA, supporting 12-bit PWM dimming and various diagnostic functions including load open circuit, short to ground, and single LED short circuit. An integrated 5V LDO powers peripherals, simplifying hardware design. This application note outlines key considerations for using the GALT62120.

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2 Core Electrical Design Considerations

2.1 Power Input Design

2.1.1 Power Supply Section (VIN Range)

The normal operating input voltage range for the chip is 4.5V–40V (DC). It is strictly forbidden to exceed 40V (**the absolute maximum rating**); exceeding this limit will cause permanent damage to the chip. Automotive power supplies fluctuate significantly (typically 9V–16V) but must handle load dumps (dropping to 4.5V) and transient spikes (up to 40V). Therefore, quadruple protection—Load Dump, Reverse Polarity, Overcurrent, and Transient Voltage—must be implemented (In typical application circuits, integrate a fuse and TVS diode for protection. For reverse polarity protection, a series diode can be added to prevent chip burnout if the power leads are reversed).

2.1.2 Power Input Filtering (Input Capacitance)

To maintain power stability, place a **10μF capacitor (for low-frequency filtering) and a 0.1μF capacitor (for high-frequency filtering)** as close as possible to the VIN pin. This configuration reduces input ripple, shortens the current loop, and minimizes power impedance drops to protect internal circuitry. To effectively minimize the loop area, these capacitors must be positioned immediately adjacent to the chip's power pins. If the trace length between the VIN pin and the automotive power interface exceeds 20cm, add a 47μF–100μF bulk capacitor (such as an electrolytic or tantalum type) at the interface to mitigate voltage ripples caused by long traces. All components must be automotive-grade to ensure stable operation from -40°C to 125°C and to prevent leakage or physical failure.

2.1.3 VLDO Voltage Output

The on-chip 5V LDO provides a regulated output of 5V ±5% with a maximum current of 50mA. It is designed to power serial communication modules and external CAN/LIN transceivers. To ensure stability and filter ripple, place a ceramic capacitor of ≥1μF as close as possible to the VLDO and GND pins. This capacitor must be present even if the LDO output is unused (no load) to prevent circuit instability; a 1μF capacitor is recommended for such cases. For long-term reliability, keep the external load at or below 45mA (maintaining a 10% safety margin) to avoid overheating. If peripheral power demands exceed 50mA, use a separate automotive-grade LDO to power high-draw components independently and prevent damage to the integrated VLDO.

2.1.4 Relationship Between Input Voltage and LED Strings

2.1.4.1 Basic Constraints

- VIN must exceed the sum of the total LED strings forward voltage (V_LED_sum) and the channel voltage drop (V_drop): VIN ≥ V_LED_sum + V_drop
- V_drop increases with higher channel currents; check the datasheet for specific values.
- If VIN - V_LED_sum < V_drop, the channel cannot maintain a constant current, which may trigger a false "Open Circuit" fault.

2.1.4.2 Diagnostic and Protection Correlation

An open circuit fault is detected when VIN - V_OUTx < V_OPEN_th_rising and VIN > CONF_ADCLOWSUPTH. The ADCLOWSUPTH must be configured correctly to prevent diagnostic errors during voltage fluctuations.

2.1.4.3 LED String Configuration Impact

Table 1 Input Voltage Requirements for LED Strings

LED String Design	Impact on Input Voltage Requirements
Increased Series LEDs	V_LED_sum increases; a higher VIN is required to satisfy VIN ≥ V_LED_sum + V_drop.
Increased Parallel Branches	Total current increases; VIN must include a margin to compensate for voltage drops caused by line loss.
High Current Applications	V_drop increases; reserve an additional margin of 0.2V – 0.3V for VIN.

2.1.5 Input Voltage Selection Methodology and Steps

2.1.5.1 Parameter Determination

- Define LED Parameters: Identify the forward voltage (Vf) and quantity (N). Calculate V_LED_sum = N × Vf_max.
- Determine Channel Current (I_OUT): (e.g., 50mA / 75mA / 100mA). Check the datasheet for the corresponding V_drop.
- Consider System Fluctuations: Automotive 12V systems typically fluctuate between 9V–16V, while 24V systems range from 18V–32V. Users must consider these extreme data.

2.1.5.2 Minimum Input Voltage Calculation

Formula: VIN_min = V_LED_sum + V_drop + V_margin

V_margin: Use 0.5V–1V for standard applications; 1V–2V is recommended for automotive cold crank or load dump scenarios to ensure VIN ≥ V_LED_sum + V_drop.

Example: For 3 LEDs (3 × 3.2V = 9.6V) at I_OUT = 50mA (V_drop = 0.5V) and V_margin = 1V: VIN_min = 9.6V + 0.5V + 1V = 11.1V. Therefore, the input should be ≥ 12V.

2.1.5.3 Maximum Input Voltage Limits

The absolute maximum VIN is 40V, with a recommended operating limit of 36V. Suppress surges (like load dumps) using TVS or Zener diodes to prevent overvoltage damage.

2.1.5.4 Margins and Derating

- Temperature Margin: Since Vf and V_drop may rise at high temperatures, increase VIN_min by an additional 0.1V–0.2V.
- Line Loss Compensation: For long wire runs, estimate the voltage drop (ΔV_line) and include it in the VIN_min calculation (typically 0.2V–0.5V).

2.1.6 Input Voltage Design Process and Key Points

2.1.6.1 Design Steps

(1) Calculate V_LED_sum = N × Vf_max (using the LED maximum forward voltage).

(2) Determine V_drop: Check the datasheet based on the target I_OUT.

(3) Calculate VIN_min: V_LED_sum + V_drop + V_margin.

(4) Verify Limits: Ensure VIN_min ≥ 4.5V and VIN_max ≤ 36V (Automotive) / 40V (Absolute limit).

(5) Set CONF_ADCLOWSUPTH = VIN_min - 0.5V (e.g., if VIN_min=11V, set to 10.5V) to avoid false low-voltage alarms.

(6) Implement Protection: Use a series fuse, a parallel TVS diode, and a π-type filter (capacitor + inductor) to suppress EMI.

2.1.7 Common Issues and Optimization Suggestions

2.1.7.1 False Open-Circuit Reports (VIN too close to V_LED_sum)

Optimization: Increase VIN or reduce the number of LEDs to ensure VIN - V_LED_sum ≥ V_drop + 0.5V.

2.1.7.2 VIN Too Low During Cold Start

Optimization: Configure Undervoltage Lockout (UVLO) or use a wide-voltage power module to keep VIN ≥ 4.5V.

2.1.7.3 Low Efficiency and High Heat at High Currents

Optimization: Lower VIN to just above V_LED_sum + V_drop to reduce heat, or switch to a switching driver to improve efficiency.

2.2 Current Setting Resistor Rref

2.2.1 Maximum Channel Current

The resistor Rref sets the maximum current for all channels based on the following formula: **IOUT(max)=1.25V/Rref×K(ref)**. This formula is calibrated by GEEHY to remain accurate across the full temperature range (-40°C to 125°C). Current accuracy is ≤± 5%, provided that Rref has 1% accuracy and a low Temperature Coefficient of Resistance (TCR). Using a 5% accuracy resistor will degrade current accuracy to ±15%, which is insufficient for automotive LED brightness consistency. While the absolute maximum single-channel current is 100mA, a 10% margin (limiting current to 90mA) is recommended to prevent overheating and maintain accuracy during long-term operation.

2.2.2 Reference Resistor Selection

Use **1% precision, low TCR (within ±50ppm/℃)** automotive-grade resistors. Rref must be placed close to the REF/GND pins, with a trace length $\leqslant$ 5 mm and a trace width $\geqslant$ 0.8 mm. Avoid routing high-current loops (like LED loads) near these traces to prevent EMI and ground bounce. Connect the Rref ground terminal directly to the chip's GND pin. Use single-point grounding to ensure it does not share a return path with the power ground.

2.2.3 Reference Resistor Power Rating

Calculate the power dissipation using $P=U^2/R$. For example, if Rref = 6.34kΩ (corresponding to approximately 100mA), $P = (0.1A)^2 \times 6340\Omega \approx 0.25mW$. A standard resistor with a 1/16W power rating is more than sufficient.

2.3 Channel Output and LED Configuration

The chip features a high-side drive architecture and supports diagnostics for Open Circuit, Short-to-GND, and Single LED Short. With a fast diagnostic response time of ≤10μs, it rapidly detects load failures. Note that single LED short-circuit diagnosis is only applicable to a single LED short; if multiple LEDs in a series string short-circuit simultaneously, software logic is required for accurate assessment.

2.3.1 Channel Usage Precautions

- Unused Channels: Must be left floating. Do not connect them to GND, power, or other signals, as this will trigger a diagnostic fault (pulling the ERR pin low and setting the FLAG_ERR register). To prevent redundant alarms, disable diagnostics for the corresponding channels in the Diagnostic Enable Register.
- Load Constraints: Do not connect inductors in series or large capacitors in parallel with the LED cathode driven by the channel.

2.3.2 PWM and LED Dimming

The PWM system offers 12-bit resolution (0.024% precision) with a configurable frequency range of 1Hz to 20kHz. Use ≥ 100Hz to avoid flicker. A range of 200Hz to 1kHz is recommended to balance visual comfort and EMC performance. Frequencies above 10kHz increase power consumption and EMI, while those below 100Hz cause visible flickering.

Dimming Methods: Supports both independent PWM dimming (per channel) and global dimming (synchronous). To achieve smooth dimming, use an exponential dimming curve rather than linear dimming to ensure smooth transitions. Recommended range is 5% to 100%. Below 5%, LED brightness may become unstable or flicker.

2.3.3 Parallel Channel Operation

The GALT62120 supports paralleling channels to achieve output currents greater than 100mA.

Paralleling is only permitted between channels on the same chip. Do not parallel across different chips.

All paralleled channels must have the same settings for current range, PWM duty cycle, and diagnostics.

Each output must be independently connected to a series current-limiting resistor. Shorting

OUTx pins together is prohibited. A small resistor must be connected in series with each OUT pin before connecting to the LED. These resistors are used for current balancing to prevent reverse current between channels, which avoids localized overheating and erroneous diagnostic faults. All resistors should be identical with 1% tolerance and low TCR. The recommended resistance range is 10–47Ω, with the specific value adjusted based on current and voltage drop requirements.

3 Serial Communication Considerations

3.1 Device Address

- The device address is determined by the pull-up or pull-down configuration of the ADDR2, ADDR1, and ADDR0 pins. These pins must not be left floating.
- Route address lines away from power lines to ensure stable logic levels during the power-up sequence.

3.2 Core Requirements for TX/RX and MCU Interface

- Level Shifting: The GALT62120 TX/RX pins operate at a 5V logic level. A 3.3V MCU requires a level shifter; do not connect them directly.
- Wiring Direction: Connect MCU_TX to GALT62120_RX and MCU_RX to GALT62120_TX. Both components must share a common ground.
- Series Resistors: Place a 22Ω–100Ω resistor (33Ω/0402 recommended) in series on each line to suppress interference and provide ESD protection.
- ESD Protection: Add one ESD diode to each RX/TX line, positioned close to the chip pins.
- Pull-up Resistor: The GALT62120_TX is an open-drain output and requires a 10kΩ pull-up resistor to 5V.
- PCB Routing: Keep RX/TX traces ≤ 10cm, wrap them with ground shielding, and maintain a distance of ≥ 2mm from high-power or motor interference lines. Use vias near pins for layer changes and avoid crossing split planes.
- Communication anomalies (packet loss, timeouts, or checksum errors) will trigger the internal watchdog, forcing the device into a fail-safe state. The watchdog timeout interval is configurable via EEPROM (1ms to 255ms). Set the timeout to 1.5 to 2 times the MCU communication cycle to avoid accidental triggers. Upon timeout, the chip executes a preset action (e.g., shutting down all channels) until communication is restored and the watchdog is reset.
- For inter-board communication, use a CAN transceiver (e.g., TJA1050-Q1) to meet automotive EMC standards (ISO 11452 and CISPR 25). Add a 120Ω, 1% precision automotive-grade resistor at both ends of the CAN bus to match impedance and reduce signal reflection.
- Register read/write operations must follow the Unlock → Operate → Verify workflow.
  ① Unlock: Write the unlock code to the LOCK register to enable configuration access.
  ② Operate: Perform the intended write or read operation.
  ③ Verify: Read the target register back to confirm the data matches, preventing errors from packet loss.

- The baud rate is configurable from 1200 bps to 1 Mbps. For automotive scenarios, 9600 bps or 19200 bps is recommended for stability. For long-distance transmission (exceeding 50 cm), use 9600 bps to minimize packet loss. The communication data format is fixed as: 8 data bits, 1 stop bit, and no parity.
- Anti-interference Measures:

  ① Isolate RX/TX pins with ground planes and keep them away from high-power components.

  ② Use shielded cables for communication lines, with the shield grounded at one end.

  ③ Implement software data verification (e.g., CRC) to prevent data corruption.

  ④ Send regular "feed the dog" (watchdog reset) commands to prevent timeouts during brief communication gaps.

4 Key PCB Layout Considerations

4.1 Prioritize Heat Dissipation

As a linear driver, the GALT62120 generates significant heat that increases with output current and input voltage. Effective thermal design is critical for reliability. The exposed bottom thermal pad must be soldered to a PCB copper plane of ≥100mm². Incorporate at least 6 thermal vias (0.8mm diameter, 2mm spacing) to connect the pad to a bottom-layer copper plane (≥200mm²). Ensure the junction temperature remains ≤ 150°C and the ambient temperature stays within the -40°C to 125°C range. In extreme environments, use a heatsink or reduce output current to prevent thermal derating.

4.2 Power Loops

Place VIN, GND, and VLDO capacitors with "zero distance" to pins (≤ 1mm). Power loop traces should be ≥ 1.5mm wide. Keep current loops ≤ 10mm to minimize impedance and ground bounce. The PCB must implement a split-ground design, separating analog ground (AGND) from power ground (PGND). The analog ground (including REF, VLDO, and communication GND pins) and the power ground (including LED load GND and VIN GND) must be tied together at a single point (star grounding) at the IC's GND pin. Cross-routing of analog and power ground traces is strictly prohibited to prevent power ground noise from interfering with sensitive analog circuitry, such as current sensing and communication.

4.3 Rref Sensitive Traces

Rref traces are sensitive analog lines. Keep them short (≤ 5mm), thick (≥ 0.8mm), and straight. Maintain ≥ 1mm spacing from switching lines, motor lines, and high-power LED traces. Do not cross ground plane splits. Connect the Rref GND terminal directly to the chip's AGND; never share a path with PGND to avoid current-sensing errors.

4.4 Serial Communication Traces

Isolate all traces with ground pouring. Surround signal lines with a ground plane (≥ 0.5mm spacing). Maintain a trace width of 0.8–1mm. Keep these ≥ 2mm away from high-power LED traces and switching power supplies. Limit trace length to 10cm. For longer distances, use a CAN transceiver. For single-ended traces, use 100Ω matching resistors to reduce reflections.

4.5 ADDR Address Configuration Traces

Position configuration resistors (ADDR0~ADDR2) close to pins (trace length ≤ 3mm). Connect the GND terminal of pull-up/down resistors to AGND to ensure accurate address identification. In multi-chip systems, keep ADDR traces separate to avoid address conflicts.

4.6 Supplemental EMC Layout

- Ensure capacitors are immediately adjacent to pins to form the shortest Power-Capacitor-GND loop.
- Use traces ≥ 1.5mm wide; keep them short and straight to minimize radiation.

- Reserve a ≥ 2mm ground border at the PCB edge for improved EMC.
- Maintain at least 1mm of clearance around the chip to isolate it from other heat-generating components.

5 Diagnostics and Fail-Safe Considerations

5.1 Fault Masking Support

Fault reporting can be masked through the CONF_MASK register series. When a fault is masked, the chip still detects the issue, but it will not update the FLAG register or trigger the ERR pin. Masking is appropriate only for non-safety-related issues (e.g., open-circuit faults on unused channels). Masking is strictly prohibited for safety-critical faults like overtemperature or supply undervoltage to ensure the system can enter a safe state immediately.

5.2 Single-Channel Diagnostic Enable

Individual channel diagnostics are controlled via the Diagnostic Enable registers (channels 0–11). Set the bit to 1 to enable diagnostics or 0 to disable them. Disable diagnostics for unused channels to prevent redundant alarms. However, be aware that disabled channels will not detect shorts, which could lead to overheating if a hardware fault exists.

5.3 Fault Actions

5.3.1 Autonomous UVLO and Over-Temperature TSD Protection (No MCU Intervention Required)

Undervoltage Lockout (UVLO) and Thermal Shutdown (TSD) are hardware-level protections that do not require MCU intervention.

If VIN drops below the threshold, the chip shuts down all channels until the voltage recovers.

If the junction temperature exceeds the safety threshold, all channels are disabled. Operation resumes only after the temperature drops below the high-temperature warning limit to prevent permanent damage.

5.3.2 Open/Short Circuit Handling (MCU Retry/Shutdown)

(1) When an LED open or short circuit is detected, the chip updates the FLAG register and pulls the ERR pin low. The MCU should execute retry logic. If the fault persists, the affected channel should be shut down.

(2) EEP_OFAF Register (Fail-Safe Configuration):

① Only Faulty Channel Off (0): Recommended for Exterior Lights (turn signals, brakes) so a single failure doesn't disable the entire lamp assembly.

② All Off (1): Recommended for Interior Lights to ensure no abnormal or uneven brightness occurs during a fault.

(3) ERR Open-Drain Pin

This pin requires an external pull-up resistor and acts as a hardware interrupt for the MCU. Active-low; it returns high automatically once the fault is cleared. Writing to the fault flag register will force the pin high, though it will return low if the fault condition still exists.

(4) Fault Diagnostic Priority

Thermal Shutdown (TSD) > UVLO > Short Circuit > Open Circuit

High-priority faults trigger protection immediately; lower-priority faults are masked until the primary issue is resolved.

6 EEPROM Configuration Considerations

The EEPROM is non-volatile memory used to store critical parameters, such as **device address, fail-safe settings, watchdog timers, default brightness, and UVLO thresholds** during power-down. This allows the chip to enter its preset operating state immediately upon power-up without MCU reconfiguration. Data retention exceeds 10 years with ≥ 1000 write/erase cycles, meeting automotive mass-production standards.

6.1 Mass Production Recommendations

- Read the ID register to confirm the Chip ID is 0x94 before programming to avoid errors.
- Always verify data after programming to prevent operation failures.
- Use automotive-grade mass-production programmers that support batch processing for better efficiency.

6.2 Fail-Safe State

Presetting fail-safe states in the EEP ensures the lighting system remains safe if the MCU goes offline, complying with ISO 26262 functional safety standards. Key parameters include: Fail-Safe Action (EEP_OFAF), Watchdog Timeout (EEP_WDT), and Default Brightness (EEP_PWM). Validate these parameters through rigorous testing before mass production to ensure they meet system safety requirements.

6.3 EEPROM Programming Precautions

- Never program the chip at high temperatures (>100°C) or low voltages (<5V), as this may cause write failures or EEPROM damage.
- Do not disconnect power during programming; doing so will corrupt the EEPROM and may brick the device.
- To change existing data, you must first erase the specific address (write 0xFF) before writing new data. Direct overwriting is not supported.

7 Software and Debugging Considerations

7.1 Power-On Initialization Sequence

(1) Wait 50ms after power-on for the chip to stabilize before attempting communication.

(2) Read the Chip ID register (0xFF); confirm the ID is 0x94 to ensure the power supply and communication lines are functional.

(3) Read the status registers to confirm no initial faults are present.

(4) Configure diagnostic thresholds, the watchdog timer, current, and PWM settings in order before enabling channels.

7.2 Configuration Sequence Standards

Follow this specific order: Diagnostic Thresholds → Watchdog → Current → PWM → Enable Outputs.

(1) Diagnostic Thresholds: Set open and short-circuit thresholds to match your specific LED load parameters.

(2) Watchdog: Configure the EEP_WDT timeout to be compatible with your MCU's communication cycle.

(3) Current: Adjust output levels by configuring the Rref resistor, Kref, and IOUT registers.

(4) PWM: Define the frequency and duty cycle for the target brightness.

7.3 Fault Handling Logic

- Periodically check the FLAG register for rapid error detection.
- Record fault types in a system log to assist in mass-production troubleshooting.
- Critical (Overtemperature/Undervoltage): Shut down all channels immediately; restart only when the fault clears. Load-specific (Open/Short): Perform a retry; if the fault persists, shut down only the affected channel.
- Once the fault condition is resolved, write to the CLR register to clear flags and resume operation.

7.4 Dimming Optimization

Avoid abrupt duty cycle transitions; apply exponential dimming for improved visual comfort. Supports 12-bit independent PWM dimming with programmable frequency up to 20kHz.

- Gradual Dimming: Implement transitions in small steps (e.g., 10ms intervals) for a smooth "breathing" effect.
- Calibration: Fine-tune PWM duty cycles during mass production to ensure brightness consistency across all 12 channels (aim for deviation ≤5%).

7.5 Mass Production Debugging and Test Standards

- Current Accuracy Test: Verify each channel at -40°C, 25°C, and 125°C to ensure output stays within ≤±5%.
- EMC Compliance: Conduct Radiated Emission, Conducted Emission, and ESD tests per ISO 11452 and CISPR 25 standards.
- Fault Simulation: Manually trigger LED open/short circuits, UVLO, and overtemperature to validate protective logic.
- Reliability Aging: Run at full load for 1,000 hours at 125°C to ensure long-term stability.
- EEPROM Audit: Randomly sample 10% of chips after batch programming to verify data integrity.

7.6 Special Debugging Precautions

Debugging is essential for verifying correct operation and troubleshooting. To prevent hardware damage and improve efficiency, focus on the following six key points:

(1) Input Voltage Debugging

The chip operates from 4.5V to 40V (DC). Strictly control the input voltage; exceeding 40V will cause permanent damage. Use an adjustable power supply. Start at 4.5V and gradually increase to 40V while monitoring the ERR pin and LED brightness. Mimic automotive fluctuations (e.g., 9V to 16V) to ensure stability. Measure input ripple with an oscilloscope to ensure it is ⩽100mVpp. If higher, optimize the layout or increase input capacitance.

(2) Communication Baud Rate Debugging

The chip supports adaptive baud rates from 1200Hz to 2MHz. Operation outside this range may cause communication issues, including packet loss, connection failure, or register read/write errors. Select the baud rate according to application requirements. 19,200 bps is recommended for debugging to balance speed and stability, while 9,600 bps is suitable for mass production with long-distance communication. Ensure the host/MCU baud rate matches the chip. If errors occur, lower the baud rate and check for interference or mismatched termination resistors.

(3) Communication Voltage Debugging

The chip's communication pins, RX (Pin 1) and TX (Pin 4), operate at a 5V level. During debugging, ensure proper level matching to avoid communication errors or chip damage. If the host or MCU uses 3.3 V logic, do not connect directly to these pins. Use a level shifter to convert 3.3 V signals to 5 V before connection. Direct connection may result in unrecognized signals, communication failure, or potential damage to the communication module. During debugging, use an oscilloscope to verify signal waveforms on the communication pins, ensuring voltage amplitude and timing meet specifications to prevent faults.

(4) Communication Tool Selection and Debugging

For initial debugging, use a PC host software with a USB-to-UART module. This setup enables quick register access, parameter configuration, and fault diagnosis, making it suitable for rapid bring-up. Ensure the correct COM port and baud rate are selected. Verify correct TX/RX cross-connection (module TX → chip RX; module RX → chip TX) and connect a common GND to avoid communication failures. After understanding basic operation, switch to MCU-based debugging by implementing firmware for register access, fault handling, and dimming control to simulate production scenarios. During MCU debugging, carefully manage communication timing to prevent configuration errors or packet loss.

(5) Chip Locking and Unlocking Debugging

The chip includes a register protection lock (LOCK register) to prevent unintended configuration changes and ensure system stability. The chip must be unlocked before any register access; otherwise, operations will be invalid and may trigger protection. Write 0x00 to the LOCK register (Address 0x61) to unlock, then wait 100μs before proceeding. After completing operations, write 0x0F to relock the register and prevent accidental modifications. If register operations fail during debugging, first confirm whether the chip is unlocked to avoid misdiagnosing communication issues.

(6) Host Computer Connection Debugging

If power, wiring, and GND are correct but the communication address is unknown, perform address scanning. The chip supports addresses 0x0–0xF (binary 0000–1111), where 0x0 is the broadcast address and not used for point-to-point communication. Therefore, valid test addresses are 0x1–0xF. When scanning, avoid rapid switching; wait 50ms between address attempts to prevent conflicts. If no address responds, recheck wiring, logic levels, and baud rate to eliminate hardware or configuration faults.

8 Revision History

Table 2 Document Revision History

Date	Version	Revision History
2026.4	1.0	● Initial version

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8. Scope of Application

The information in this document replaces the information provided in all previous versions of the document.